INTEL740(TM) GRAPHICS ACCELERATOR FULL FEATURED REFERENCE CARD

+12V = 12V ANALOG UNLESS OTHERWISE SPECIFIED

VCC = 5V DIGITAL UNLESS OTHERWISE SPECIFIED

VCC3 = 3.3V DIGITAL UNLESS OTHERWISE SPECIFIED

VDDQ = 3.3V AGP POWER SUPPLY

VCC_CORE = VOLTAGE SUPPLIED TO THE INTEL740 CHIP CORE

GND = DIGITAL GND

Title: Cover Sheet		
Size: C	Document Number: Intel740(TM) Graphics Accelerator Reference Card	Rev: 2.1
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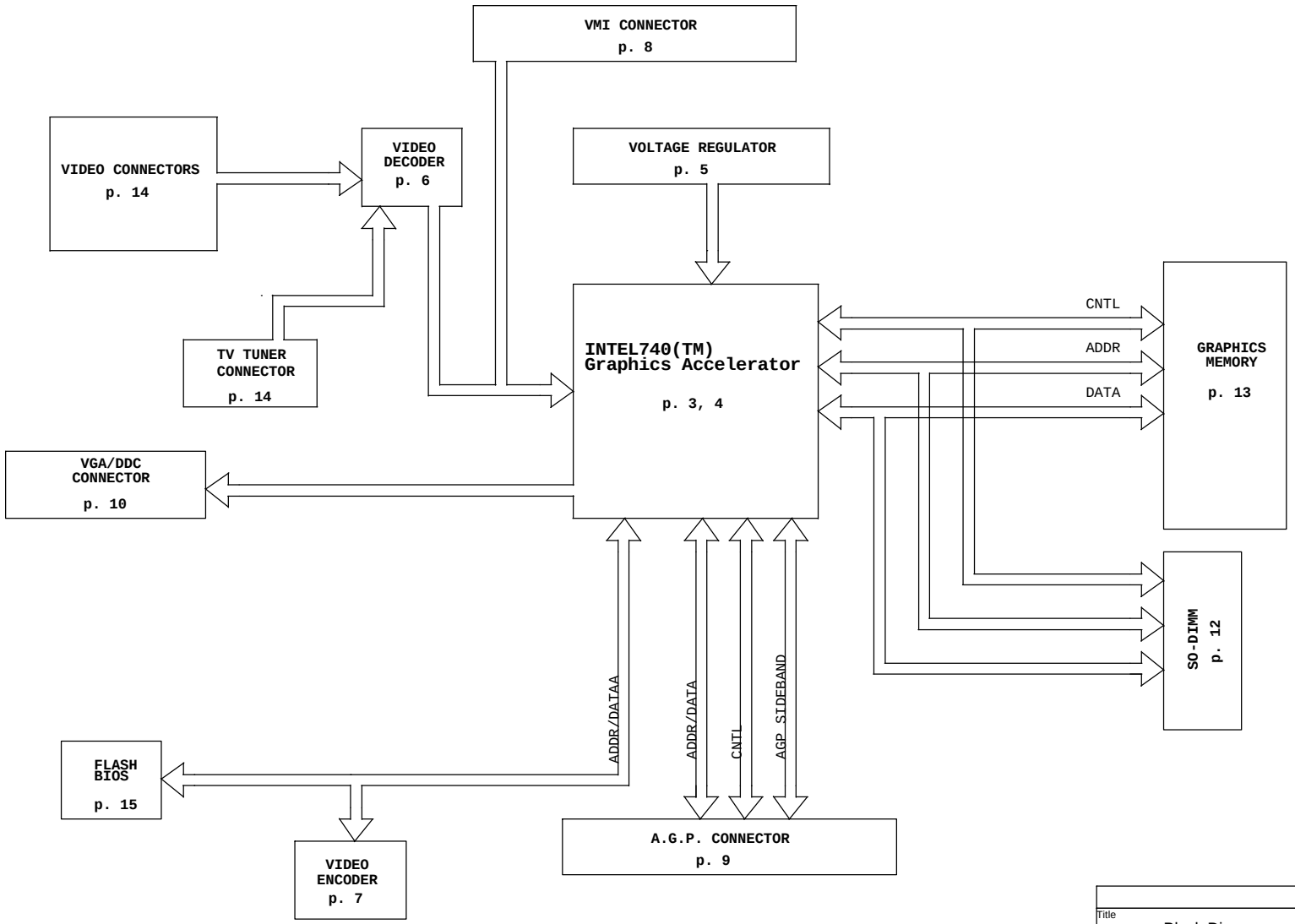

Title	Block Diagram	
Size B	Document Number Intel740(TM) Graphics Accelerator Reference Card	Rev 2.1
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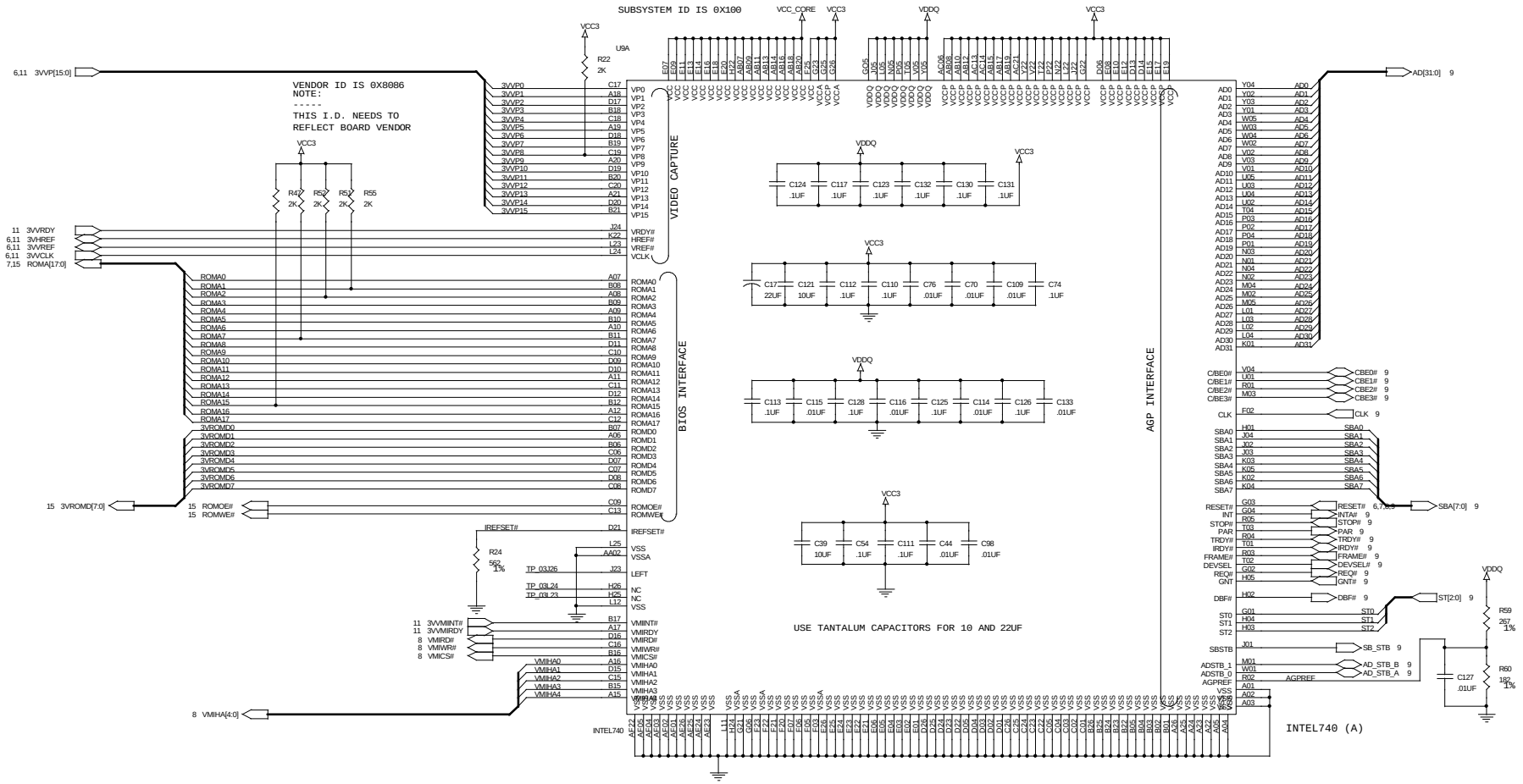

Title	Intel740(TM) Graphics Accelerator(A)		
Size: C	Document Number: Intel740(TM) Graphics Accelerator Reference Card		Rev: 2.1
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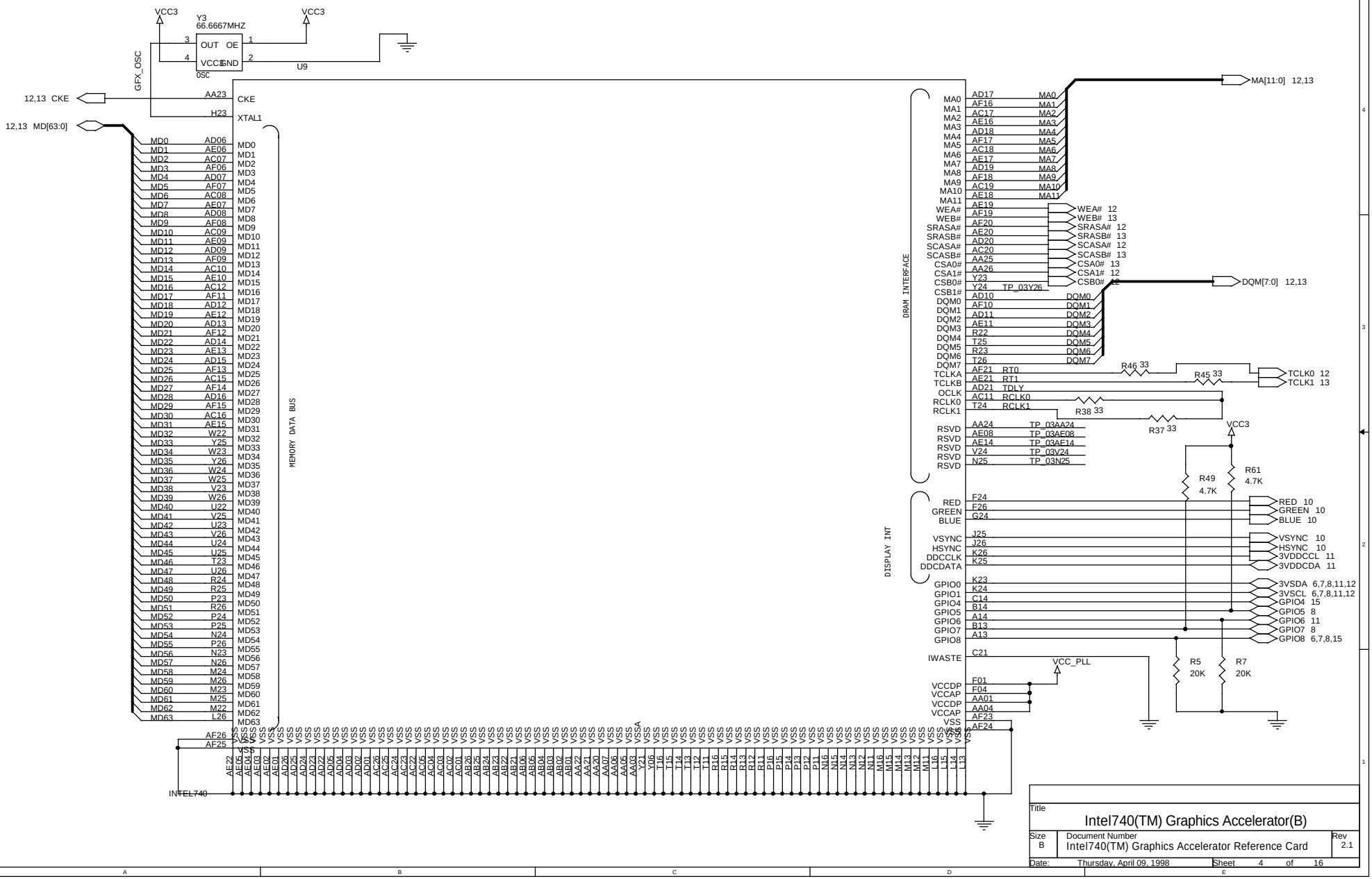

Title	Intel740(TM) Graphics Accelerator(B)	
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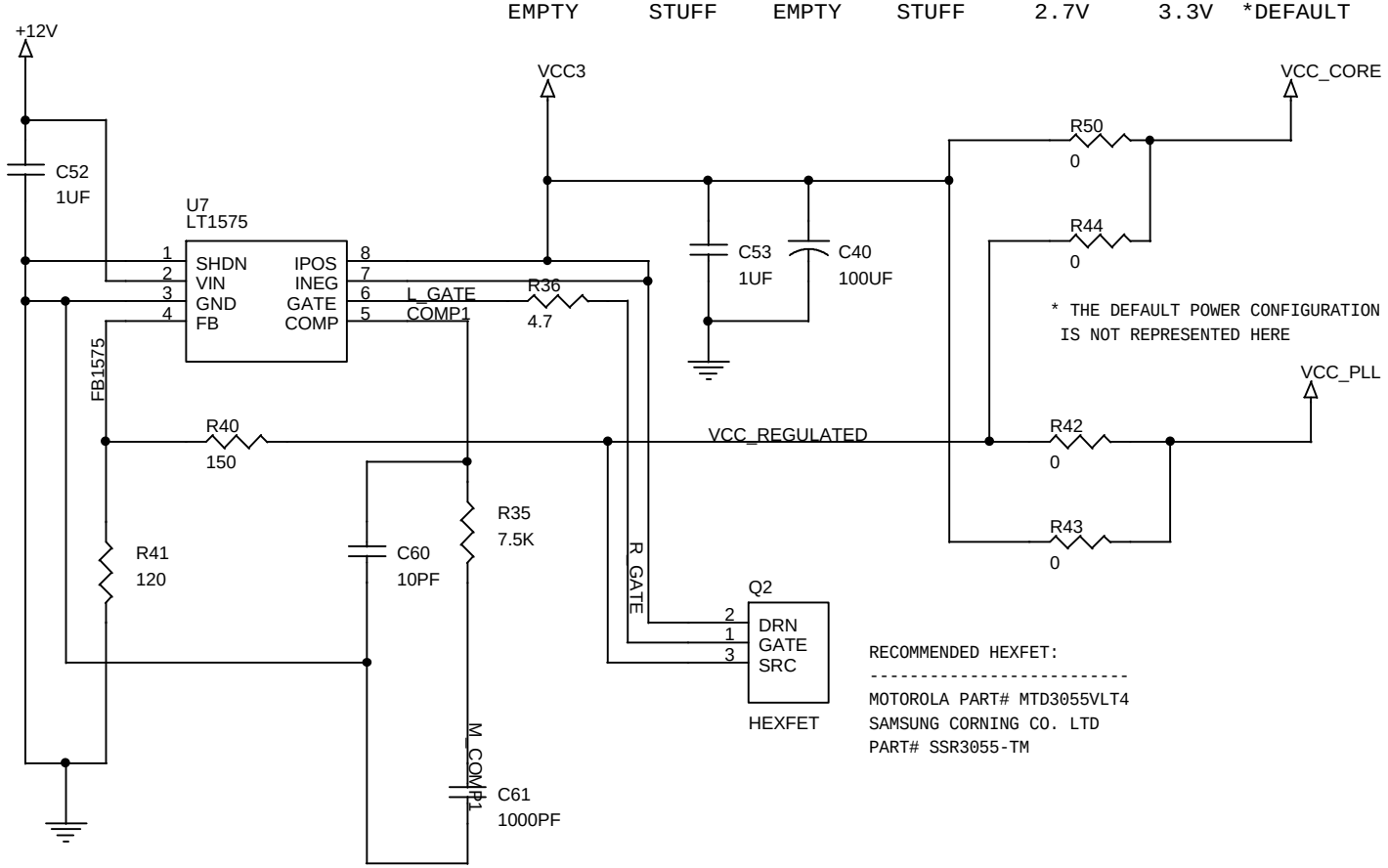
POWER CONFIGURATION*

R50	R44	R42	R43	CORE	PLL	
STUFF	EMPTY	STUFF	EMPTY	3.3V	2.7V	
EMPTY	STUFF	STUFF	EMPTY	2.7V	2.7V	
STUFF	EMPTY	EMPTY	STUFF	3.3V	3.3V	
EMPTY	STUFF	EMPTY	STUFF	2.7V	3.3V	*DEFAULT



NOTE:

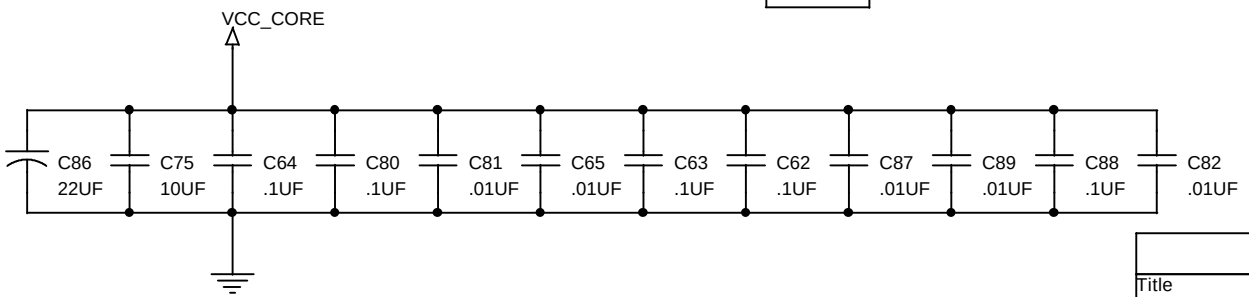
THE NET CONNECTING C60 TO C61
SHOULD BE CONNECTED DIRECTLY
TO PIN 3 OF THE LT1575 DUE TO
THE GROUND BOUNCE SENSIVITITY OF
THE LT1575 COMPENSATION PIN

TO VARY THE OUTPUT VOLTAGE, REPLACE
R40 WITH THE FOLLOWING VALUES TO
ACHIEVE THE VARIOUS OUTPUT
VOLTAGES:

R40	VOUT
150	2.7V
160	2.8V
170	2.9V
180	3.0V

RECOMMENDED HEXFET:

MOTOROLA PART# MTD3055VLT4
SAMSUNG CORNING CO. LTD
PART# SSR3055-TM



Title
Voltage Regulator

Size	Document Number	Rev
A	Intel740(TM) Graphics Accelerator Reference Card	2.1

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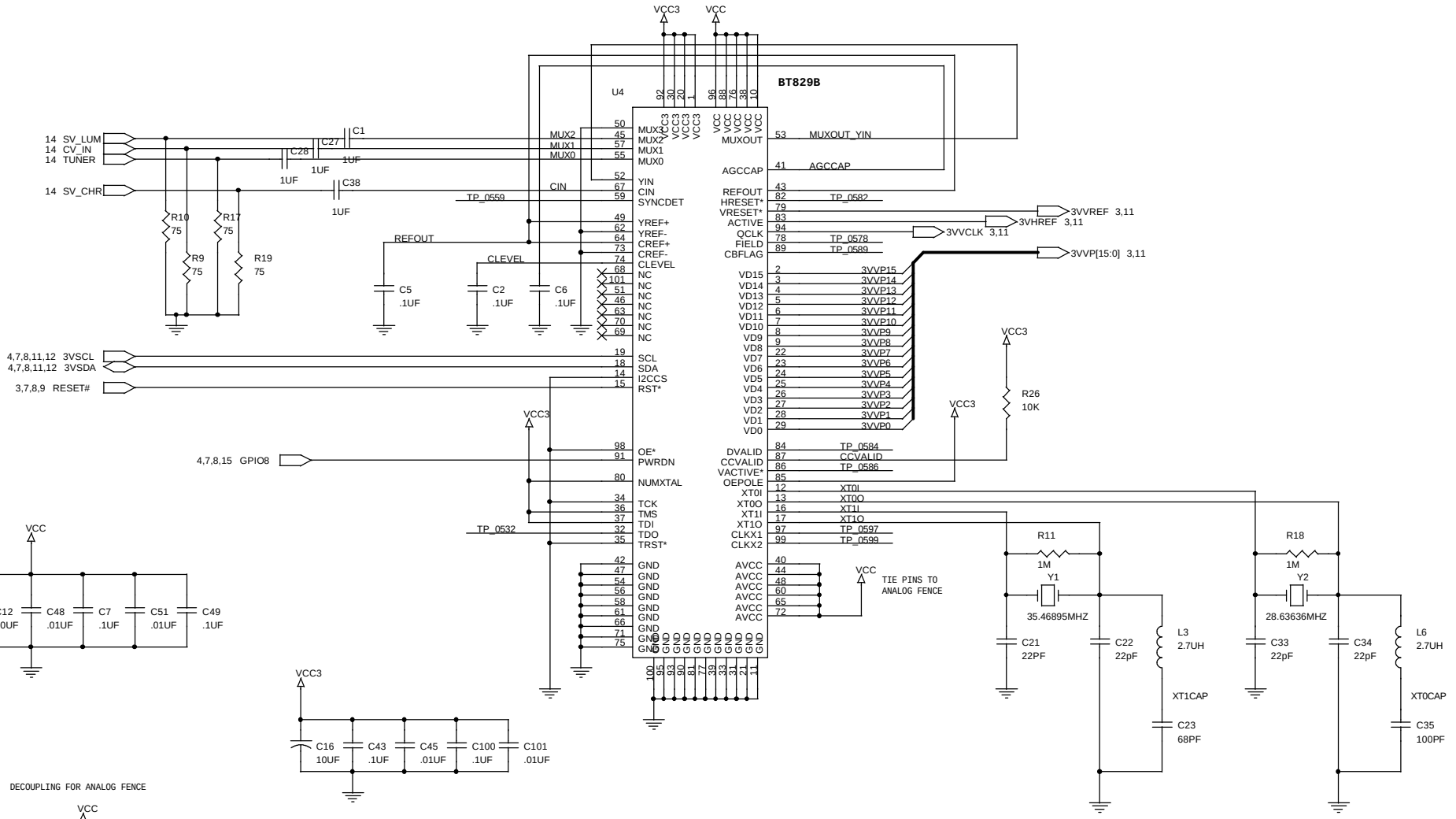
NOTE: ANALOG PLANE NEEDS TO BE FENCED FROM THE DIGITAL PLANE



Title	Bt829B Video Decoder	
Size B	Document Number Intel740(TM) Graphics Accelerator Reference Card	Rev 2.1
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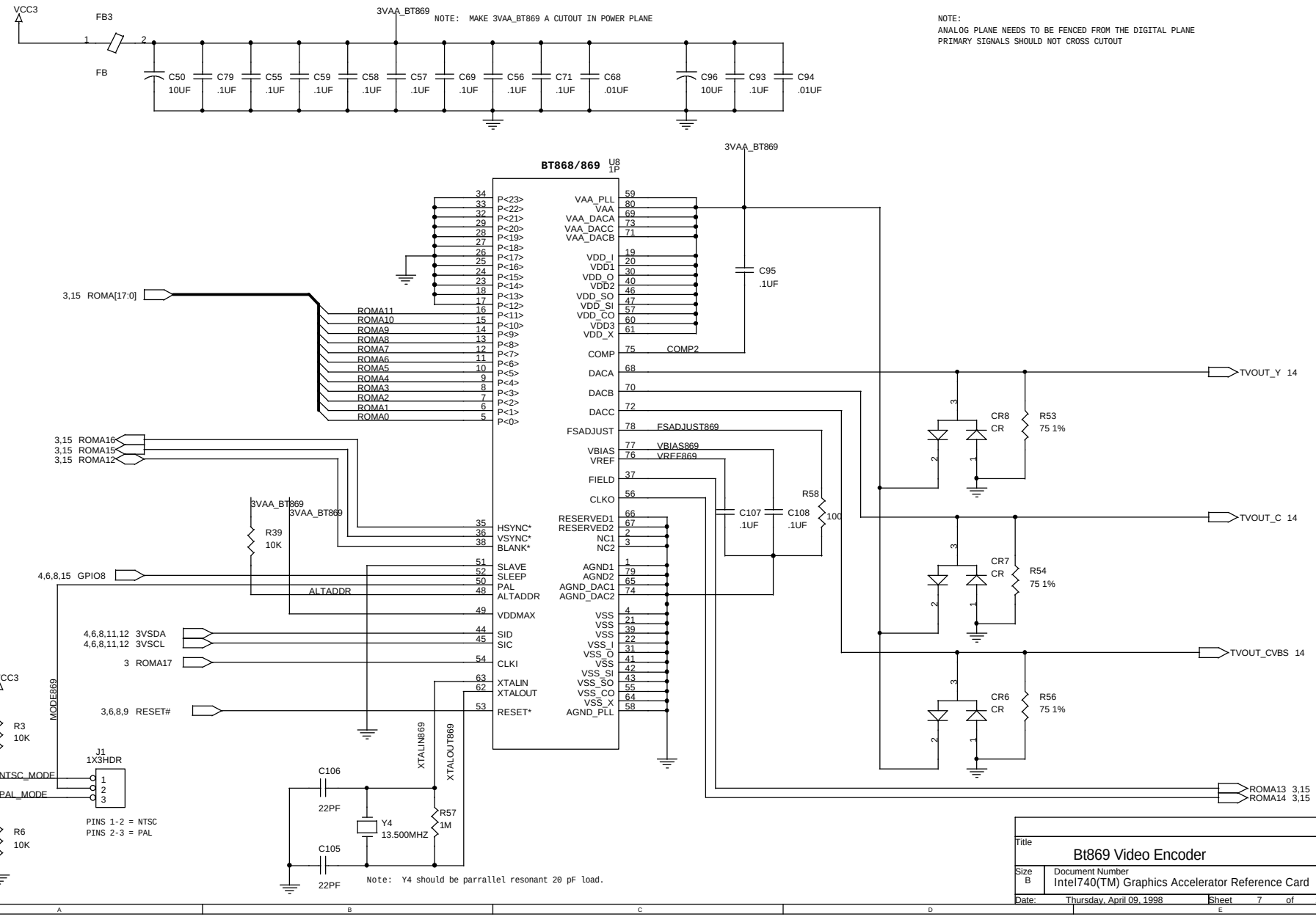

Title	Bt869 Video Encoder	
Size B	Document Number Intel740(TM) Graphics Accelerator Reference Card	Rev 2.1
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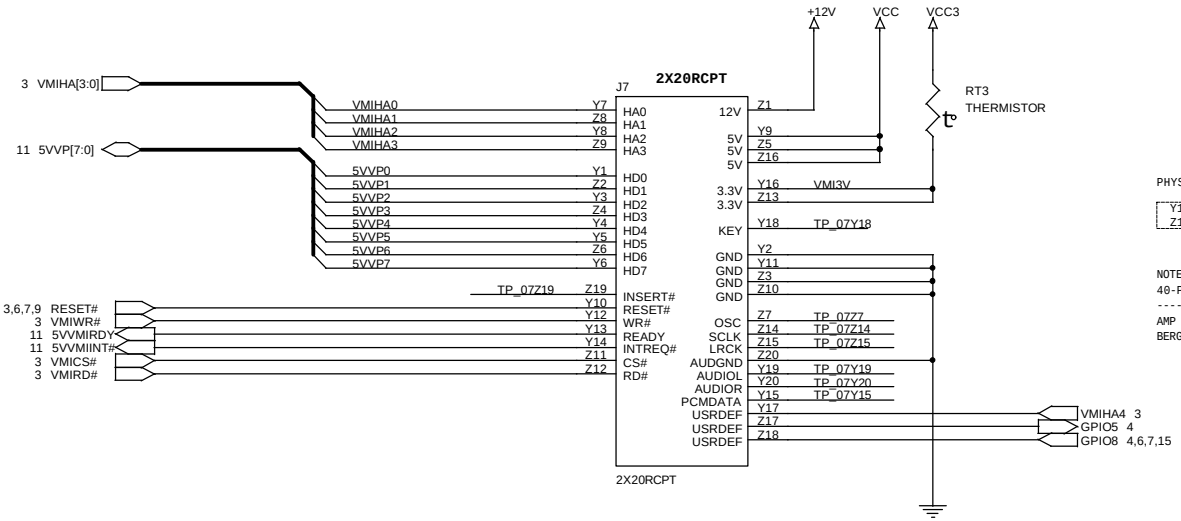
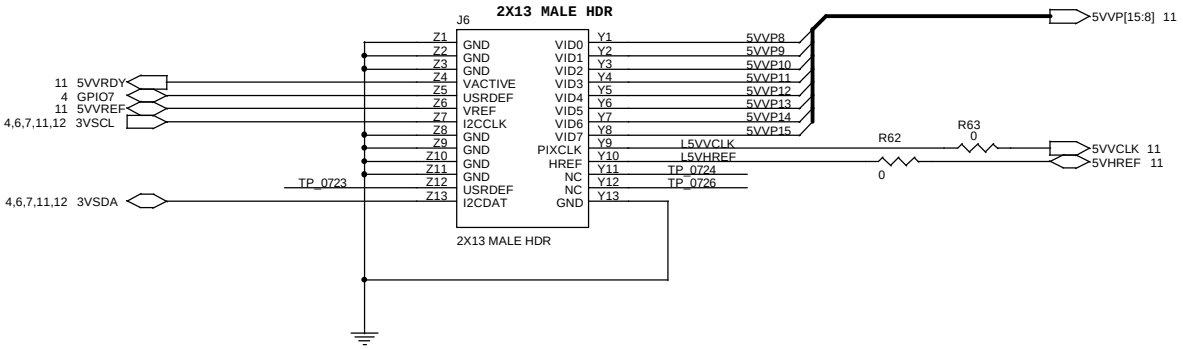


PHYSICAL PINOUT VIEW OF THE 40 PIN HEADER (COMPONENT SIDE)

Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15	Y16	Y17	Y18	Y19	Y20
Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	Z9	Z10	Z11	Z12	Z13	Z14	Z15	Z16	Z17	Z18	Z19	Z20

NOTE:
40-PIN FEMALE HEADER RECOMMENDED PARTS

AMP PART# 2-535598-3
BERG PART# 68683-320



PHYSICAL PINOUT VIEW OF THE 26 PIN HEADER (COMPONENT SIDE)

Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13
Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	Z9	Z10	Z11	Z12	Z13

NOTE:
26-PIN MALE HEADER RECOMMENDED PARTS

AMP PART# 1-103186-3
BERG PART# 67997-426

Title	VMI Video Connectors	
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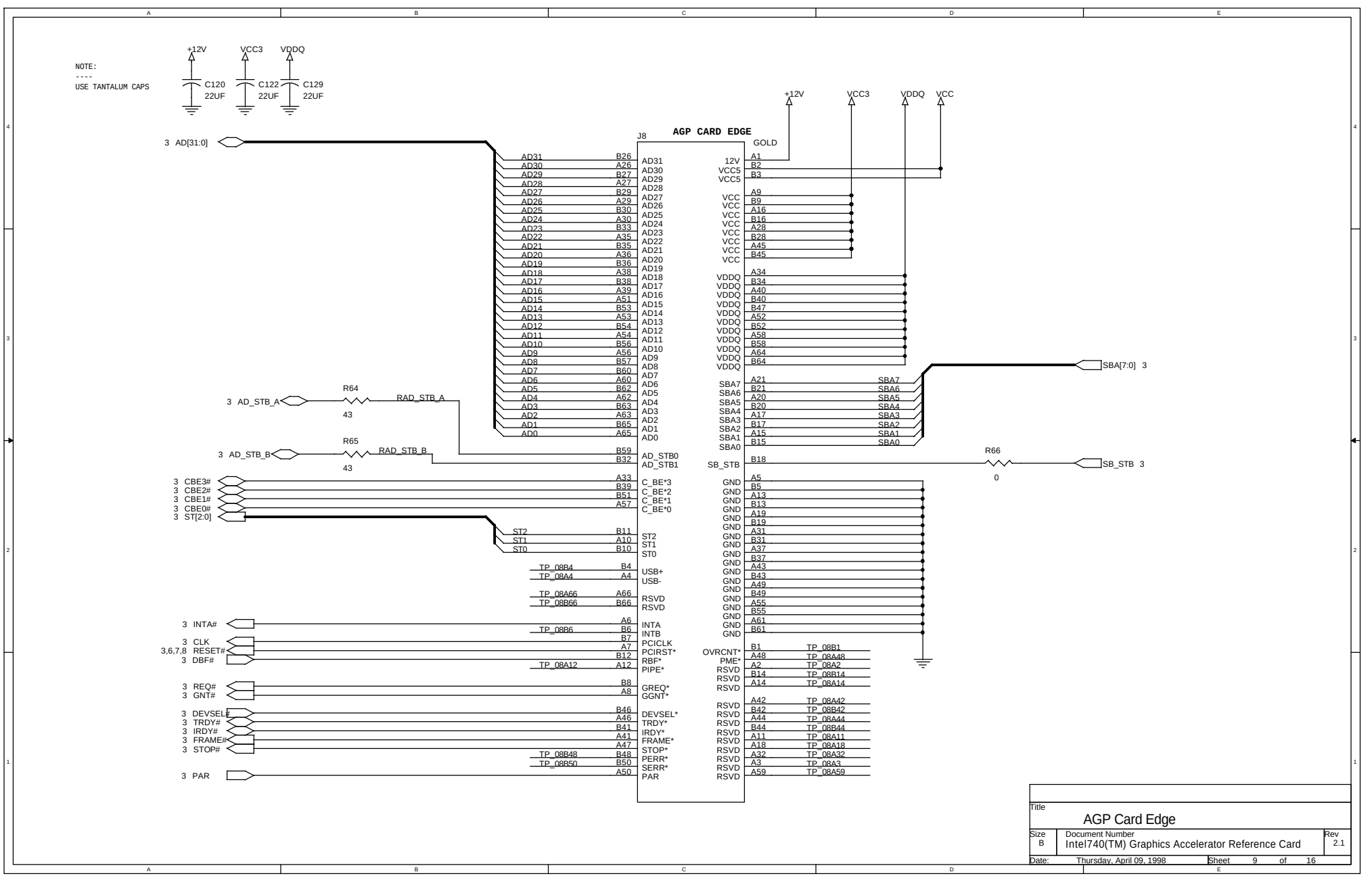

Title	AGP Card Edge		
Size B	Document Number Intel740(TM) Graphics Accelerator Reference Card		Rev 2.1
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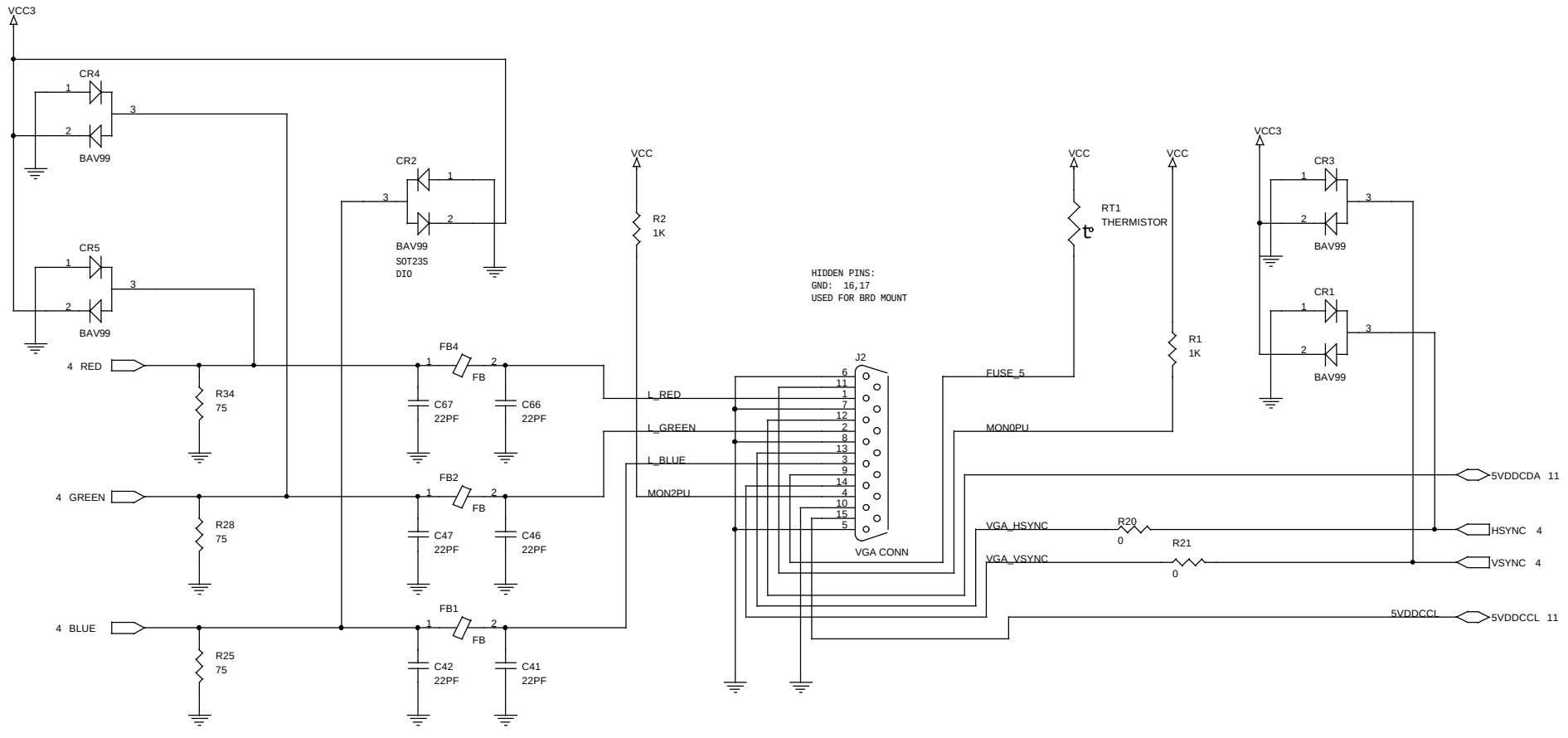

Title	VGA Connector	
Size B	Document Number Intel740(TM) Graphics Accelerator Reference Card	Rev 2.1
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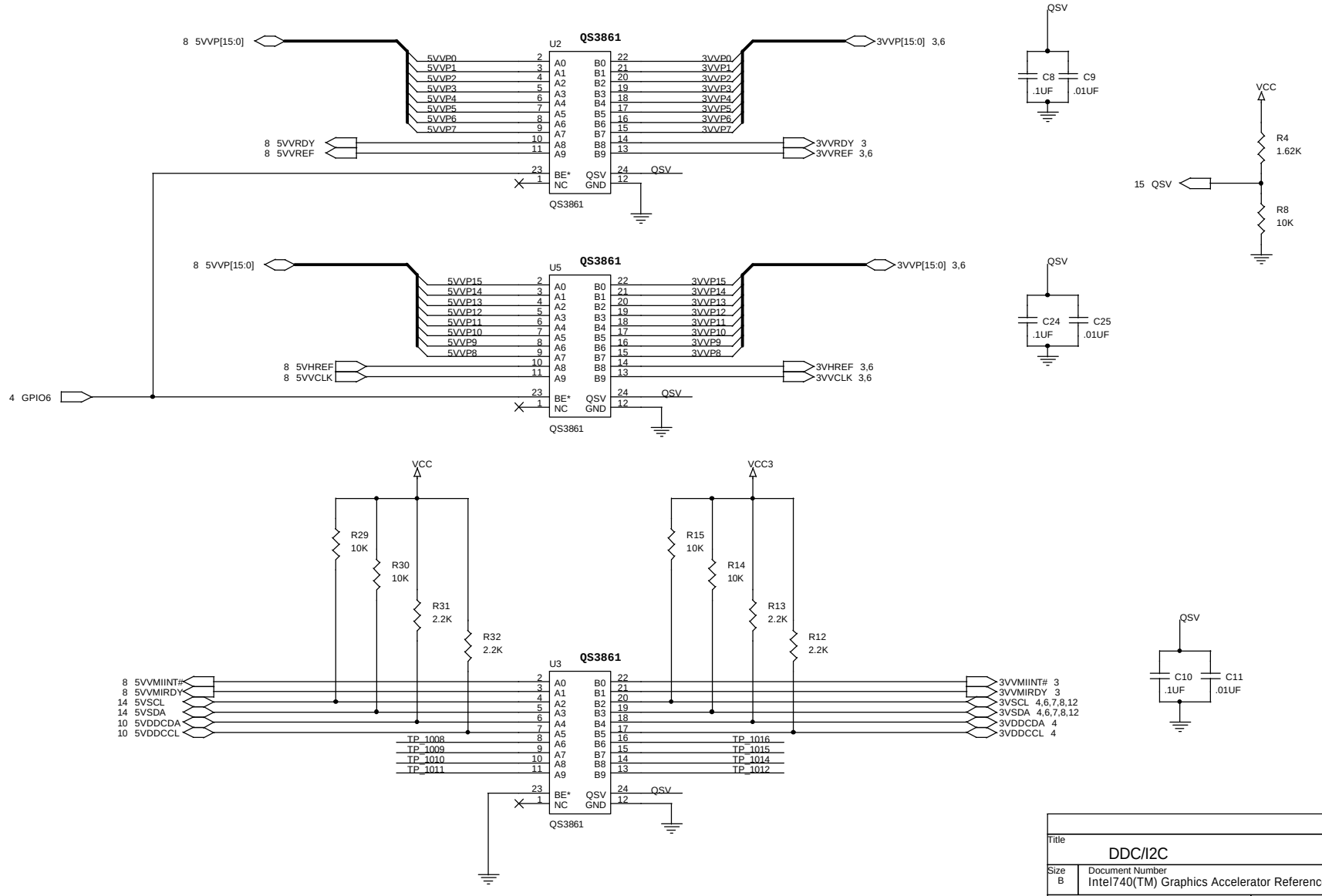
QS3861
U2
8 5VVP[15:0]
5VVP0
5VVP1
5VVP2
5VVP3
5VVP4
5VVP5
5VVP6
5VVP7
3VVP[15:0] 3,6
3VVP0
3VVP1
3VVP2
3VVP3
3VVP4
3VVP5
3VVP6
3VVP7
8 5VVRDY
8 5VVREF
3VVRDY 3
3VVREF 3,6
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9
BE* NC
QSV GND
QS3861
QSV
C8 .1UF
C9 .01UF
VCC
R4 1.62K
15 QSV
R8 10K
U5
8 5VVP[15:0]
5VVP15
5VVP14
5VVP13
5VVP12
5VVP11
5VVP10
5VVP9
5VVP8
3VVP[15:0] 3,6
3VVP15
3VVP14
3VVP13
3VVP12
3VVP11
3VVP10
3VVP9
3VVP8
8 5VHREF
8 5VVCLK
3VHREF 3,6
3VVCLK 3,6
4 GPIO6
C24 .1UF
C25 .01UF
VCC
VCC3
R29 10K
R30 10K
R31 2.2K
R32 2.2K
R15 10K
R14 10K
R13 2.2K
R12 2.2K
U3
8 5VVMIINT#
8 5VVMIRDY
14 5VSCL
14 5VSDA
10 5VDDCDA
10 5VDDCCL
3VVMIINT# 3
3VVMIRDY 3
3VSCL 4,6,7,8,12
3VSDA 4,6,7,8,12
3VDDCDA 4
3VDDCCL 4
TP_1008
TP_1009
TP_1010
TP_1011
TP_1016
TP_1015
TP_1014
TP_1012
C10 .1UF
C11 .01UF
Title
DDC/I2C
Size B
Document Number
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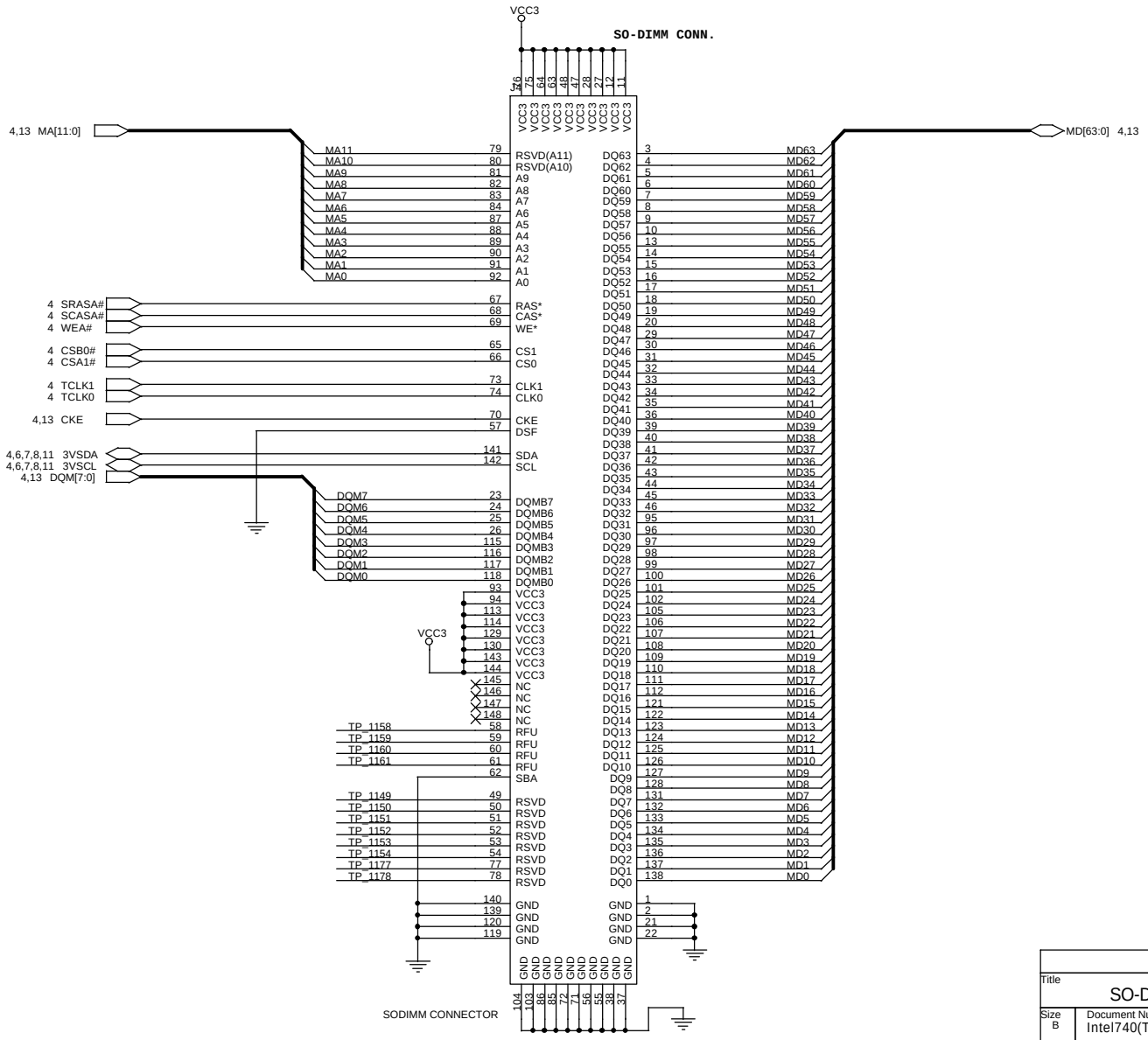

Title	SO-DIMM Connector	
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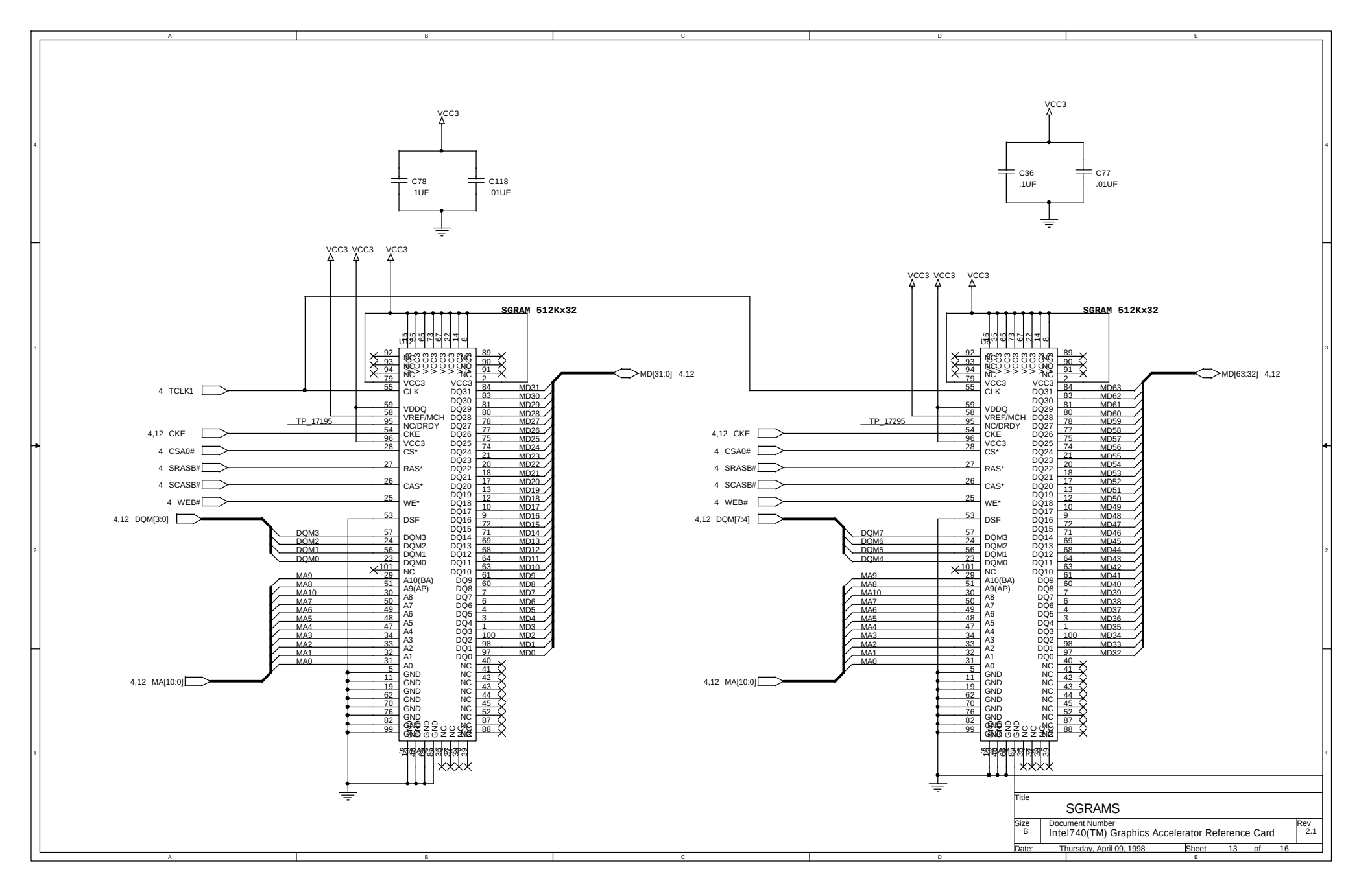
VCC3
C78
.1UF
C118
.01UF
C36
.1UF
C77
.01UF
SGRAM 512Kx32
MD[31:0] 4,12
MD[63:32] 4,12
4 TCLK1
4,12 CKE
4 CSA0#
4 SRASB#
4 SCASB#
4 WEB#
4,12 DQM[3:0]
4,12 DQM[7:4]
4,12 MA[10:0]
TP_17195
TP_17295
Title
SGRAMS
Size B
Document Number
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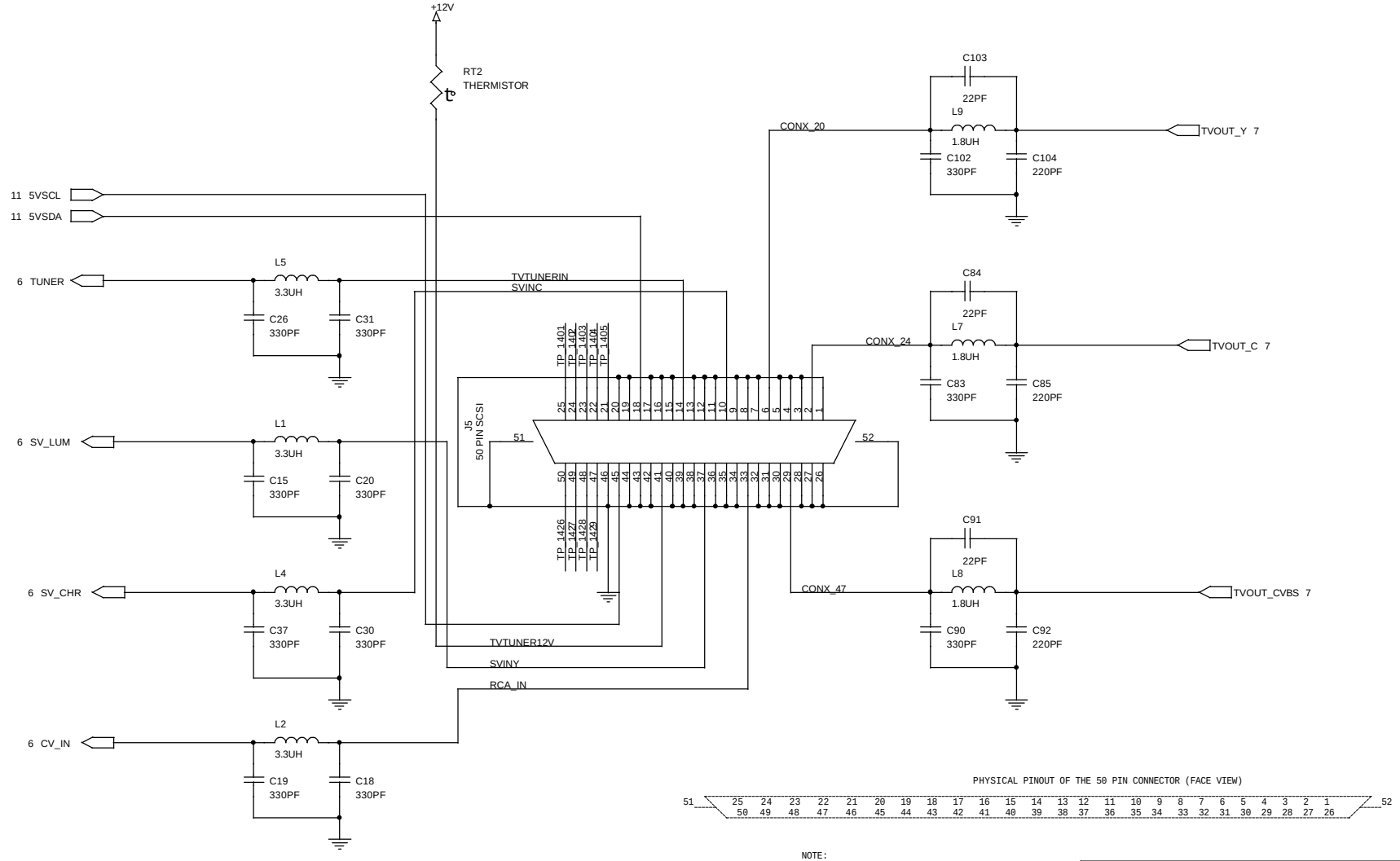
+12V
RT2
THERMISTOR
11 5VSCL
11 5VSDA
6 TUNER
6 SV_LUM
6 SV_CHR
6 CV_IN
L5
3.3UH
C26
330PF
C31
330PF
L1
C15
C20
L4
C37
C30
L2
C19
C18
TVTUNERIN
SVINC
TVTUNER12V
SVINY
RCA_IN
J5
50 PIN SCSI
51
52
TP_1401
TP_1402
TP_1403
TP_1404
TP_1405
TP_1426
TP_1427
TP_1428
TP_1429
C103
22PF
L9
1.8UH
C102
330PF
C104
220PF
CONX_20
TVOUT_Y 7
C84
L7
C83
C85
CONX_24
TVOUT_C 7
C91
L8
C90
C92
CONX_47
TVOUT_CVBS 7
PHYSICAL PINOUT OF THE 50 PIN CONNECTOR (FACE VIEW)
51 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 52
50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26
NOTE:
50-PIN FEMALEL SCSI CONNECTOR RECOMMENDED PART

AMP PART# 787170-5
Title
Video Connector
Size B
Document Number
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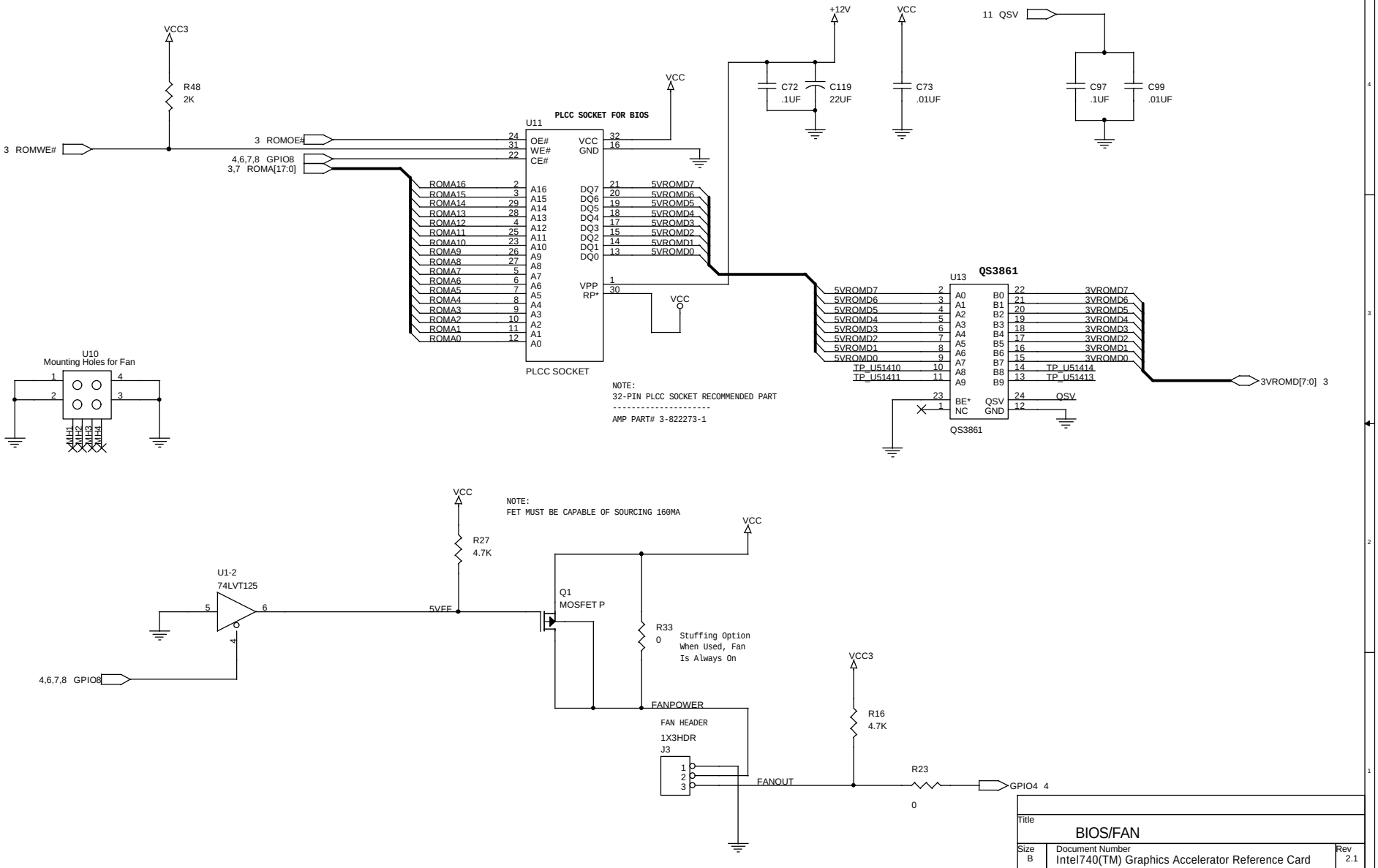

Title	BIOS/FAN	
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1.1 REVISIONS

PULL-DOWN REISITOR ON GPIO4 REMOVED
SIGNAL GPI08 ADDED TO VMI 2X20 HEADER ON PIN Z18
FAN FAIL SIGNAL REMOVED FROM QSWITCH
OE# ON INTEL740(TM) GRAPHICS ACCELERATOR OSCILLATOR PULLED HI TO 3.3V
MEMORY ADDRESSES 8,9 AND 10 FROM INTEL740 CONNTECTED TO 9,10 AND 8 OF SODIMM CONNECTOR, RESPECTIVELY
GPIO4 PULLED UP TO 3.3V THRU 4.7K RESISTOR

1.2 REVISIONS

MEMORY ADDRESSES 8,9 AND 10 FROM INTEL740(TM) GRAPHICS ACCELERATOR CONNECTED TO 8,9 AND 10 OF SODIMM CONNECTOR, RESPECTIVELY

POWER SUPPLY VDDQ3 CHANGED TO VDD

1.3 REVISIONS

REMOVED 1UF CAP BETWEEN PIN 1 AND GND OF LT1575 ON P.4
ADDED 1UF CAP TO VCC3 NEAR PIN 1 OF HEXFET ON P.4
REPLACED 220UF CAP WITH 100UF CAP ON P.4
LAYOUT NOTE ADDED TO P.4

1.4 REVISIONS

SIGNAL NAMES L_RED, L_GREEN, L_BLUE CHANGED TO L_RED, L_GREEN AND L_BLUE, RESPECTIVELY, ON P.9
SIGNAL NAMES VGA_SHYNC AND VGA_VSYNC CHANGED TO VGA_HSYNC AND VGA_VSYNCE ON P.9
NET NAMES CONX_20, CONX_24 AND CONX_47 ADDED TO P.13
MOUNTING HOLES FOR FAN ADDED TO P.14
FOR HIDDEN PINS OF FAN MOUNTING HJOLES ADDED TO P.1
AGND CHANGED TO GND GLOBALLY
AVCC CHANGED TO VCC GLOBALLY
ON HIDDEN PINS OF BT829ALV REMOVED FROM P.5
PROPERTY OF BT829ALV ADDED, HIDDEN PINS DESIGNATED AS ANALOG_GND CONNECT TO GND
POWER NOTES CHANGED ON P.1 TO REFLECT AGND AND AVCC REMOVAL

1.41

THE 4 GND RINGS OF FAN MOUNTING HOLES BROUGHT OUT EXTERNALLY P.14
THE 4 NC MOUNTING HOLES ARE STILL LEFT AS HIDDEN

1.42

0 OHM RESISTOR ADDED TO GPIO4 LINE ON P.14
UNSTUFFED 0 OHM RESISTOR ADDED BETWEEN DRAIN AND SOURCE OF PMOSFET ON P.14
PINOUT CHANGED ON INTEL740(TM) GRAPHICS ACCELERATOR ON PINS SPARE2, SPARE1, LEFT, VSYNC, HSYNC, VREF, AND VCLK.
NEW PIN'S ARE H25, H26, J23, J25, J26, L23, & L24 RESPECTIVELY ON P.3.
NO OTHER PINS AFFECTED.

1.43

ADDED DISCLAIMERS TO P.1
ADDED NOTE REGARDING HIDDEN PINS OF VGA CONNECTOR ON P.1
AGP NOTE CHANGED TO A.G.P. ON P.8
COMPATIBILITY NOTE REMOVED FROM TITLE ON P.10
512X32 SGRAMS NOTE CHANGED TO JUST SGRAMS
BUTEO TV ENCODER NOTE CHANED TO BT869 VIDEO ENCODER
POWER PINS NOTE CHANGED TO HIDDEN POWER PINS ON P.1
BT829B NOTE CHANGED TO BT829ALV VIDEO DECODER ON P.1 & 5
ADDED NOTE ON P.4 REGARDING VARYING THE OUTPUT VOLTAGE OF REGULATOR
SIGNAL NAME XTL1 CHANGED TO XT1I ONP.5, PIN16 OF BT829ALV
SIGNAL NAME XT10 CHANGED TO XT1O ON P.5, PIN17 OF BT829ALV

1.44

NOTE ON HIDDEN VCC PINS FOR BT829ALV CHANGED, PIN 28 TO 38 ON P.1
POWER PLANE VDD CHANGED TO 3VAA_BT829 FOR 3 PROTECTION DIODES ON P.6
SIGNAL NAMES L_GATE, R_GATE, COMP1 M_COMP1 ADN FB1575 ADDED TO P.4
SIGNAL NAMES XT1CAP AND XT0CAP ADDED TO NETS ON P.5
SIGNAL NAMES XTALIN869, XTALOUT869, M_COMP2, COMP2, FSADJUST869, VBIAS869 AND VREF869 ADDED TO NETS ONP.6
SIGNAL NAME VMI3V ADDED TO NET ON P.7
SIGNAL NAME FANPOWER ADDED TO NET ON P.14

1.45

SIGNAL NAME CCVALID ADDED TO P.5

1.46

SIGNAL NAME GFX_OSC ADDED TO P.3
SIGNAL NAME MODE869 ADDED TO P.6, PIN 50 OF BT869
SIGNAL NAME PAL_MODE ADDED TO 1X3HDR ON P.6
SIGNAL NAME NTSC_MODE ADDED TO 1X3HDR ON P.6

1.46

NOTE STATING NEED A 10% VERSION CREATED REMOVED FROM P.8
POWER SUPLY VCC3 CHNAGED TO VCC ON C123 ON P.14
POWER SUPPLY VCC3 CHANGED TO VCC ON BIOS SKT ON P.14
SIGNAL NAME 5VSDA CHANEGD TO 3VSDA ON U9.Z13 ON P.7
AGP CONNECTOR NOTES ON PINS CHANGED ON P.8, NO SIGNAL NAMES WERE CHANGED ON THE CONNECTOR
NAMES GAD[31:0] CHANGED TO AD[31:0], SMB1 AND SMB0 CHANGED TO RSVD
GAD_STB0 AND GAD_STB1 CHANGED TO AD_STB0 AND AD_STB1, RESPECTIVELY
GC-BE*3,2,1,0 CHANGED TO CBE*3,2,1,0 RESPECTIVELY
GSTOP*, GPERR*, AND GPAR CHANGED TO STOP*, PERR*, SERR* AND PAR, RESPECTIVELY

1.5 REVISIONS

C39, C41, C42, & C44 CHANGED TO 15PF ON P.5, NO PACKAGE SIZE CHANGE NEEDED
SIGNALS XT1CAP AND XT0CAP RELOCATED SINCE XTAL FILTERS CHANGED ON P.5
L3 AND L4 ON P.5 CHANGED TO 4.7UH NAD LOCATION IN XTAL FILTER CIRCUIT CHANGED
PIN 36, 37, 80, & 85 CONNECTED TO VCC3 INSTEAD OF VCC ON THE BT829ALV ON P.5
R20 ON P.5 NOW CONNECTS TO VCC3 INSTEAD OF VCC
C20, C22, C23 AND C26 ON P.5 CHANGED FROM 0.1UF TO 1UF. THESE ARE THE AC CAPS TO MUX INPUTS.
THIS REQUIRED A PACKAGE SIZE CHANGED FROM 0805 TO 1206.
VCC CONNECTION TO PIN 59 OF BT829B (P.5) DELETED. WIRE LEFT OPEN AND RENAMED TP_0559.
REMOVED NOTE NEAR PIN 59 OF BT829B (P.5) WHICH STATED TIE TO ANALOG FENCE
DELETED R13, R18 & R19 FROM P.5 OF SCHEMATICS.
REPLACED C38 ON P.5 WITH A SHORT. THE SIGNALS MUXOUT AND YIN WERE THUS REMOVED AND RENAMED AS ONE SIGNAL MUXOUT_YIN
SIGNAL NAME BROMWE# REMOVED FROM P.14
GPIO7 SIGNAL NAME AND NET REMOVED FROM P.14 AND CONNECTED TO PIN Z5 OF THE 2X13 HDR ON P.7
ROMWE# SIGNAL NO LONGER USES 74LVT125 ON P.14 BUT CONNECTS DIRECTLY TO BIOS PIN 31
PULL-UP RESISTOR TO VCC3, R13, ADDED ON P.14 AND CONNECTED TO THE ROMWE# SIGNAL
SIGNAL NAME TP_0709 REMOVED FROM 2X13 HDR ON P.7 AND CHANGED TO GPOI7
R63 ON P.6 CHANGED FROM 75 TO 100 OHMS
R62 REMOVED AND REPLACED BY A SHORT ON P.6
SIGNAL NAME M_COMP2 REMOVED FROM P.6
C112 REMOVED FROM P.6
BT829ALV NAME CHANGED TO BT829B ON P.1 AT 2 PLACES AND P.5 AT 2 PLACES
BT868, 869 TV OUT NOTE ON P.2 CHANGED TO VIDEO ENCODER
AGP CONNECTOR NOTE ON P.2 CHANGED TO A.G.P. CONNECTOR

1.6 REVISIONS

ALL REFERENCE DESIGNATORS CHANGED
HIDDEN POWER PINS NOTATION ON P.1 CHANGED

1.61 REVISIONS

50 PIN VIDEO PINOUT CHANGED ON P.13, PIN 1 NEEDED TO CHANGE DUE TO PAD PATTERN DEFINITION
DIAGRAM SHOWING THE PHYSICAL PINOUT OF THE 50 PIN VIDEO CHANGED ACCORDINGLY ON P.13
NOTE ON P.4 WHICH STATED ...R10 WITH THE ... CHANGED TO ...R35 WITH THE...
NOTE ON P.4 WHICH STATED ...R10 VOUT... CHANGED TO ...R35 VOUT...
NOTE ON P.4 WHICH STATED ...C12 TO C11... CHANGED TO ...C60 TO C61...
C21, C22, C33, & C34 ON P.5 CHANGD TO 22PF CAPS, SAME PACKAGE SIZE
L3 AND L6 ON P.5 CHANGED TO 2.7UH, SAME PACKAGE SIZE
C23 ON P.5 CHANGED TO 68PF, SAME PACKAGE SIZE
C35 ON P.5 CHANGED TO 100PF, SAME PACKAGE SIZE
REF DESIGNATOR FOR C16 ON P.4 CHANGED TO C40
REF DESIGNATOR FOR C40 ON P.5 CHANGED TO C16

1.7 REVISIONS

10K PULL-DOWN RESISTOR TO GND ADDED TO GPIO8 SIGNAL ON P.3
PINS F01, AA01, F04 & AA04 REMOVED FROM HIDDEN PINS OF INTEL740(TM) GRAPHICS ACCELERATOR CONNECTED TO VCC3 ON P.1
PINS F01, AA01, F04 & AA04 ADDED TO INTEL740(TM) GRAPHICS ACCELERATOR SYMBOL AND CONNECTED TO SIGNAL VCC_PLL ON P.3
VCC2 NOTES ON P.1 CHANGED TO VCC_CORE TO REFLECT THE CORE POWER SUPPLY CHANGED ON P.4
HIDDEN INTEL740(TM) GRAPHICS ACCELERATOR PINS WHICH WERE CONNECTED TO VCC2 CHANGED TO CONNECT TO VCC_CORE
THE FOLLOWING ARE HIDDEN PINS WHICH WERE CONNECTED TO VCC2 CHANGED TO CONNECT TO VCC_CORE
E07, E09, E11, E13, E14, E16, E18, H22, AB07, AB09, AB11, AB13, AB14, AB16, AB18, AB20
OUTPUT OF REGULATOR SIGNAL NAME CHANGED TO VCC_REGULATED FROM VCC2 ON P.4
TWO 0 OHM RESISTORS ADDED, BOTH CONNECTED TO VCC_CORE, ONE CONNECTED TO VCC_REGULATED, THE OTHER VCC3 ON P.4
ANOTHER TWO 0 OHM RESISTORS ADDED, SMALLER PACKAGE, BOTH CONNECTED TO VCC_PLL
ONE CONNECTED TO VCC_REGULATED, THE OTEHR VCC3 ON P.4
ADDED ON P.4 TO DESCRIBE THE RESISTOR STUFFING OPTIONS FOR CORE AND PLL POWER
CHANGED PMOSFET ON P.14 FROM A 3 PIN DEVICE TO A 4 PIN DEVICE, THE MIDDLE PIN (2) AND THE TAB (4) ON TEH PHYSICAL DEVICE ARE ELECTRICALLY THE SAME, BOTH ARE DRAINS
VCC2 POWER SYMBOL CONNECTED TO DECOUPLING CAPACITORS ON P.4 CHANGED TO VCC_CORE'
VCC2 NO LONGER EXISTS

1.8 REVISIONS

REFERENCE DESIGNATORS CHNAGED ACCORDING TO PHYSCIAL LOCATION ON BOARD BY LAYOUT COMPANY

1.9 REVISIONS

NOTES ON REFERENCE DESIGNATORS ON PAGE 1 UPDATED
NOTE REGARDING 0 OHM STUFFING OPTIONS ON P.4 CHANGED
NOTE REGARDING DEFAULT POWER CONFIGURATION ADDED TO P.4
HIDDEN RULE ON AD<31:0> CHANGED TO HIDDEN

2.0 REVISIONS

OSC Y3 VALUE CHANGED TO 66.6667MHz (p.4)

2.1 REVISIONS

Made Power Pins Visible and changed names to match the Datasheet,
Swapped pin numbers for WEA# and WEB# (p.3,4)

Made power pins visible (p.6)

Changed VCC3 voltages on part to 3VAA_BT869,
Changed R58 to 100 ohms (p.7)

Pin A3 on AGP connector disconnected from Ground,
changed VDD to VDDQ (p.9)

Made power pins visible (p.11)

Made power pins visible, Changed Clock Routing (p.12)

Made power pins visible (p.13)

Added descriptive text to Fan control, made
power pins visible (p.15)

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